REMARKS

This application has been reviewed in light of the Office Action dated March 4, 2008. Claim 7 has been amended. Claims 1-2 and 4-21 are now pending in the application. Claim 3 remains canceled without prejudice.

The Examiner's reconsideration of the rejection in view of the following remarks is respectfully requested.

By the Office Action, claims 1, 2, 4-13, 15-18 and 20-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Japanese Publication, JP 2001-30511 (hereinafter 'Murai') in view of U.S. Publication No. 2002/0084967 (hereinafter 'Akimoto').

Murai is directed to a circuit including transistors 11, 13 and 14 (see, e.g., Murai FIG. 6). As illustrated in FIG. 6, for example, transistor 11 transmits signals from line 1 to the gates of transistors 13 and 14. In addition, the gate of transistor 11 is controlled by signals from line 51, which determines when signals from line 1 are transmitted to the gates of transistors 13 and 14. However, the circuits illustrated in the figures of Murai do not disclose or remotely suggest that the timing of the routing of data signals to the gates of switching transistors are dependent upon at least one input that is connected to a switching transistor through which the input may be routed to a pixel element. As depicted in the Figures of Murai, line 51, which controls when signals are transmitted to the gates of transistors 13 and 14, is not connected to either transistor 13 or 14. Thus, the timing of the routing of signals to the gates of transistors 13 and 14 is not dependent upon at least one input that is connected to a switching transistor for routing to a pixel element.

Similarly, Akimoto does not disclose or suggest a data signal that is routed to the gates of switching transistors with a timing dependent on at least one input that is connected to a switching transistor through which the input may be routed to a pixel element. As shown in FIG. 25 of Akimoto, Akimoto describes a circuit including a transistor 1 that transmits signals from line 12 to the gate of transistor 87. Similar to Murai, discussed above, line 11 is connected to the gate of transistor 1 to control when signals are transmitted to the gate of transistor 87. Further, transistor 87 is connected to input line 92 and a capacitor 88 is connected between the gate of transistor 87 and a terminal of transistor 87 (see, e.g. Akimoto, FIG. 25).

Akimoto fails to disclose, however, that the timing of the routing of signals to the gates of transistor 87 is dependent upon at least one input that is connected to a switching transistor through which the input may be routed to a pixel element. As illustrated in FIG. 25, gate line 11 is not connected to transistor 87. Accordingly, Akimoto fails to disclose or suggest a data signal routed to a gate of a switching transistor with predetermined timing in dependence on at least one input that is connected to a switching transistor through which the input may be routed to a pixel element.

In contrast to Murai and/or Akimoto, claim 1 includes the feature of a data signal routed to a gate of a switching transistor with predetermined timing in dependence on at least one input that is connected to a switching transistor through which the input may be routed to a pixel element. Claim 1 of the present application recites:

> A device comprising an array of pixels, each pixel including a pixel element and being associated with a switching circuit, wherein the switching circuit is for selectively routing one of at least two inputs to the pixel element, comprising at least first and second switching transistors connected between a respective one of the at least two inputs and the pixel element, wherein each switching transistor is controlled by a data signal applied to the gate of the transistor, wherein the data signal for each switching transistor is routed to the gate of the switching transistor with predetermined timing determined in dependence on the data waveform of at least one of the inputs, and wherein a capacitive connection is provided between the gate of at least one of the switching transistors and a common output node of the switching transistors.

Thus, claim 1 is believed to be patentable over Murai and Akimoto, taken singly or in combination, at least because neither reference discloses or renders obvious the feature of a data signal routed to a gate of a switching transistor with predetermined timing in dependence on at least one input that is connected to a switching transistor through which the input may be routed to a pixel element. Moreover, claims 2 and 4-9 are also believed to be patentable over Murai and/or Akimoto due at least to their dependencies from claim 1.

Similar to claim 1, claim 10 recites, inter alia:

> A device comprising an array of pixels, each pixel including a pixel element and being associated with a switching circuit, wherein the switching circuit is for selectively routing one of at least two inputs to the pixel element, comprising at least first and second switching transistors connected between a respective one of the at least two inputs and the pixel element, wherein each switching transistor is controlled by a data signal applied to the gate of the transistor, wherein the data signal for each switching transistor is routed to the gate of the switching transistor with predetermined timing determined in dependence on the data waveform of at least one of the inputs . . . .

As discussed above, neither Murai nor Akimoto disclose or render obvious the feature of a data signal routed to a gate of a switching transistor with predetermined timing in dependence on at least one input that is connected to a switching transistor through which the input may be routed to a pixel element. Therefore, claim 10 is believed to be patentable over the references. Furthermore, claims 11-13 and 15-18 are also believed to be patanble over Murai and/or Akimoto due at least to their dependencies from claim 10.

In addition, claim 20 recites, inter alia:

> applying data signals to the gates of at least first and second switching transistors connected between a respective one of the at least two inputs and the pixel element to turn on a selected one of the first and second switching transistors and turn off the other of the first and second switching transistor, thereby routing the respective input to the pixel element, wherein the timing of application of the data signals is selected in dependence on the signals on at least one of the two inputs,

As stated above, Murai and/or Akimoto fail to disclose or render obvious the feature of a data signal routed to a gate of a switching transistor with timing in dependence on at least one input that is connected to a switching transistor through which the input may be routed to a pixel element. Accordingly, claim 20 is believed to be patentable over the references.

Moreover, claim 21 is believed to be patentable due at least to its dependency on claim 21. As such, withdrawal of the rejection is respectfully requested.

By the Office Action, claim 14 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Murai in view of Akimoto and further in view of PCT Publication No. WO 01/40857 (U.S. Publication No. 2002/0158993) (hereinafter 'Murai '993') and claim 19 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Murai in view of Akimoto and further in view of U.S. Patent No. 5,105,288 (hereinafter 'Senda').

While the Applicant respectfully disagrees with these rejections, claims 14 and 19 depend from claim 10 and are believed to be in condition for allowance at least due to this reason. Reconsideration of the rejection is earnestly solicited.

In view of the foregoing amendments and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to applicant's representatives Deposit Account No. 14-1270.

Respectfully submitted,

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